UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/717,359	11/18/2003	Sudip K. Nag	X-1376 US	8181

24309 7590 07/13/2006

XILINX, INC
ATTN: LEGAL DEPARTMENT
2100 LOGIC DR
SAN JOSE, CA 95124

EXAMINER	
SIEK, VUTHE	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 07/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/717,359	NAG, SUDIP K.	
	Examiner	Art Unit	
	Vuthe Siek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 April 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,6-9 and 13-20* is/are rejected.

7)☒ Claim(s) *3-5 and 10-12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/717,359 and amendment filed on 11/4/2005. Claims 1-20 remain pending in the application.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-2, 6-9 and 13-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Rahut et al. (6,766,504).

4. As to claims 1, 8, 15-16, 17-18 and 19-20, Rahut et al. teach a method and apparatus for identifying routing for interconnects for an integrated circuit (IC) design having a predefined routing topologies. Fig. 1 shows placement and routing of an IC design that includes routing topologies. Fig. 4 shows a system comprises router and timing engine used to place and route the circuit design based on template connections and analyze the circuit design using the timing parameters. For each logic level, interconnects (template connections) are identified as shown in Fig. 1. Each logic level comprises one or more template connections as shown in Fig. 1. Timing information associated with each connection is determined (delays types associated with each connection are determined; col. 2 lines 39-61; MinPathSlack, described in col. 6-7).

Rahut teaches sets of independent connections (sets of (AB), (BC, BD) and (CE, CF, DG), where each connection has determined delay (critical delay or non-critical delay) (Col. 6 lines 1-2; col. 5 lines 26-46). This clearly teaches that the timing information includes sets of timing attributes for one or more interconnects in each logic level of routing topology, where each set of the timing attributes being associated with one of a plurality of locations within the IC in which the circuit design is placeable (Fig. 1, each node or object A to G represents a circuit design that is placeable). Slacks (timing parameters) for each interconnect (connection) are formed based on the sets of the timing attributes in order to determine critical paths and non-critical paths (at least see summary). Based on the timing information, Rahut et al. teach all critical connections (template connections) within a selected logic level can be routed at a time (col. 3 lines 64-67).

5. As to claims 2 and 9, Fig. 1 shows the routing topology comprising a source and at least one sink for each connection, wherein each set of timing attributes comprising a signal delay between each source-sink pair (propagation delay). Connections in each logic level represent timing independent connections, all connections within a selected logic level can be routed at a time, without a need for intermediate timing update. Delays types are described (col. 1 lines 17-34; MinPathSlack described in col. 6-7).

6. As to claim 6-7 and 13-14, Rahut et al. teach the IC is PLDs, each of the plurality of locations is defined by a group of programmable logic blocks. Note that the PLDs comprise a group of programmable logic blocks. The circuit design comprises at least one clock net (col. 1).

Allowable Subject Matter

7. Claims 3-5 and 10-12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art of record does not teach or fairly suggest forming timing parameters comprising selecting a minimum delay in response to the signal delay for each source-sink pair in each set of timing attributes; and selecting a maximum delay in response to the signal delay for each source-sink pair in each set of timing attributes.

Remarks

8. Applicant argued that Rahut does not teach or suggest determining sets of timing attributes for a routing topology of a template, where each set of timing attribute is associated with one of a plurality of locations within an IC in which the circuit design is placeable. Examiner disagrees. Rahut clearly teach routing topology (portion of a routing network of placeable circuit design) (Fig. 1A). The routing topology Fig. 1A comprising placeable circuit design (objects A to G, the circuit design A to G is placed at each assigned location as shown in Fig. 1A). Then routing is performed to connect between objects. Fig. 1A or 1B show a plurality of sets (AB), (BC, BD) and (CE, CF, DG) of independent connections, where each connection is associated with delay (timing attribute) (col. 6 lines 1-16). Thus, Rahut clearly teaches determining sets of timing attributes for the routing topology, each set of timing attributes being associated with one of a plurality of locations within the IC in which the circuit design is placeable. Therefore, it is not true that Rahut teaches only one set of timing attributes. Since,

Rahut teaches sets of independent connection as shown in Fig. 1A or 1B (col. 6 lines 1-15), where each set has determined delays (critical delays, non-critical delays for the routing topology) for the routing topology (col. 5 lines 14-46). Applicant also argued that Rahut does not concern placing of circuit design. It is not true. Before routing process can be performed, circuit designs (objects A to G of Figs. 1A or 1B) must be placed and they must be placed at available or assigned locations. Shown in Fig. 1A or 1B just only a portion of a circuit design being placeable in an integrated circuit.

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

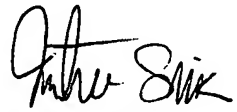
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vuthe Siek whose telephone number is (571) 272-1906.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vuthe Siek



VUTHE SIEK
PRIMARY EXAMINER